REMARKS

Claims 1 through 3 and 6 through 22 remain pending in the present case.

SPECIFICTION

102 REJECTIONS

In the above referenced Office Action, Claims 1-7, 9, and 11-20 are rejected under 35 USC 102(e) as being anticipated by Dodd et al. (U.S. Patent 6,530,006). Applicant has reviewed the Dodd et al. reference and, for the following rationale, Applicant respectfully reasserts that the present invention is not anticipated nor rendered obvious by the Dodd et al. reference.

In regards to Claims 1, 11 and 17, Applicant respectfully contends that the Dodd et al. reference fails to teach an interface and memory array on a single substrate with interfaces operating at different rates. In the Response section, the present Office Action alleges it is clear from the Dodd et al. reference that the system interface at one side of the information configuration core 120 communicates with system input clock 10 of the memory controller at one rate and the memory interface at the other side of information core 120 communicates with the memory array at another rate, the delay locked loop, phase locked loop, or delay chain to compensate/control the different in "rate' by phase alignment in order to prevent clock skew. To the extent the Dodd et al. reference may mention an input clock applied to an embedded clock circuit from which an output

clock is supplied [Col. 3, lines 5 – 7], Applicant respectfully assert the Dodd et al. reference does not teach communicating at a first communication rate and a second communication rate. Furthermore, Applicant again respectfully reasserts the Dodd et al. reference teaches away by indicating the frequency and phase of the input and output signal are the same [Col. 5, lines 27 – 30]. The present Office Action indicates the "Examiner disagrees". Applicant respectfully asserts the Dodd et al. reference indicates "When the PLL is "locked", the frequency and phase of the output signal are the same as those of the input signal" (Emphasis added) [Col. 5 lines 28 – 30].

The present Office Action goes on to allege that "It is inherent in a conventional system, the system clock is always higher than that the memory clock." Applicant again respectfully contends that a rejection indicating the Dodd et al. reference inherently teaches a system clock is always higher than the memory clock is legally improper. Anticipation by inherent disclosure is appropriate only when the references disclose prior art that must necessarily include the unstated limitation. Transclean Corp. v. Bridgewood Services Inc., 290 F3.d 1364, 1373, 62 USPQ2d 1865 (Fed Cir. 2002). Applicant respectfully asserts that the indication in the Dodd et al. reference that it is required that each component operates with the same interface voltage and frequency [Col. 1, lines 38 – 40] contradicts the Examiners allegation that in a conventional system the system clock is always higher that the memory clock and also teaches away from the present invention. It is impermissible to disregard portions of a prior art reference that teach away from an invention. Hughes Aircraft Co. v. United States, 15 Cl. Ct. 267, 275, 8 USPQ2d 1580, 1583 (Cl. Ct. 1988). In addition, Applicant respectfully reasserts the Dodd et al. reference teaches away by indicating the same input and output frequency.

The present Office Action also indicates "... Dodd clearly states that "there is a need for a system and method to provide a memory system that would not only provide reliable transmission and reduce clock insertion and propagation delay, but also would not require each component to operate with the same interface voltage and frequency" (emphasis added)". Applicant respectfully asserts the acknowledgement in the present Office Action that a there is a need for a system that would not require each component to operate with the same interface voltage and frequency seems to teach away from conventional systems always inherently have different frequencies because if the conventional systems always have different frequencies there would not be a need for them to require each component to operate at the same frequency if the conventional systems already operated at different frequencies. Appellant respectfully asserts the present invention rates do not flow undeniably and irrefutably from the express disclosures of the Dodd et al. reference, it is only present by virtue of the intervening step of human perception awareness and understanding (a product of reasoning and insight). See Hughes Aircraft Co. v. United States, 15 Cl. Ct. 267, 271, 8 USPQ2d 1580, 1583 (Cl. Ct. 1988). Appellant respectfully asserts that the possibility or even probability that the Dodd et al reference impliedly teaches two rates is not enough. Motorola, Inc. v. Interdigital Technology Corp. 930 F. Supp. 952, 970 (D. Del. 1996).

To the extent the Dodd et al. reference may mention external (discrete) buffers are utilized to allow different voltages and frequencies to be used for the memory controller 110 and memory devices 130 – 145 and 170 – 185 [Col. 3 lines 43 – 45], Applicant respectfully asserts the Dodd et al. reference does not teach a system interface for communicating with a system controller at a first communication rate, and a memory array interface for communicating with a memory array at a second

communication rate, wherein the memory array is included on the same substrate as said high speed serial memory interface system. Applicant respectfully asserts that the mention in Dodd et al. of allowing different voltages and frequencies to be used for the memory controller 110 and memory devices 130 – 145 and 170 – 185 is directed to frequencies that are different or "vary" from one value to another but whatever the difference or variance both the memory controller 110 and memory devices 130 – 145 and 170 – 185 vary in unison. For example, both the memory controller and memory devices can operate at 100 hertz or both operate at 150 hertz. Applicant respectfully asserts that this interpretation is supported by the remainder of the Dodd et al. reference indication that the phase lock loop drives the output to the input signal and the frequencies are the same.

Even if the Dodd et al. reference mention of different frequencies can be interpreted in another manner, Applicant respectfully asserts that the Dodd et al. reference still teaches away from the present invention anyway by indicating that external (discrete) buffers [Col. 3, lines 40 – 45] are utilized to allow different frequencies rather than buffers on a single substrate.

The present Office Action appears to rely on a second reference Wikipedia to support the rejections under 35 USC 102(e) as being anticipated by Dodd et al. (U.S. Patent 6,530,006). To the extent the Wikipedia may mention many electronic systems use internal clocks which are required to be phase-aligned to and/or frequencies multiples of some external clock (emphasis added) [first sentence of page one], Applicant respectfully asserts the Wikipedia reference of and/or indicates Wikipedia recognizes that a phase lock loop can be utilized for phase-alignment without there

necessarily being a frequency multiple or difference. Applicant respectfully s that the Wikipedia reference supports Applicant's contention that a rejection indicating the Dodd et al. reference inherently teaches a system clock is always higher than the memory clock is legally improper. Anticipation by inherent disclosure is appropriate only when the references disclose prior art that must necessarily include the unstated limitation. Transclean Corp. v. Bridgewood Services Inc., 290 F3.d 1364, 1373, 62 USPQ2d 1865 (Fed Cir. 2002). In addition, Applicant respectfully asserts the Wikipedia reference indicates "sometimes the reference clock is the same frequency as the clock driven through the clock distribution, other time the distributed clock may be some rational multiple of the reference" (emphasis added) [first full sentence page 4]. Applicant respectfully asserts that the Wikipedia acknowledgement that sometimes the reference clock is the same frequency as the clock driven through the clock distribution indicates that the Dodd reference does not inherently (necessarily) teach difference frequencies.

Applicant respectfully asserts that to the extent the Delay Lock Loop [Column 4, line 42 to Col. 5 line5], Phase Lock Loop [Col. 5, lines 6-32] and Delay Chain [Col. 5, lines 45 –56] of the Dodd et al. reference are utilized to adjust or correct phase shifts and/or clock skew the Dodd et al. reference indicates the phase shifts are due to propagation delays [Col. 3, lines 47 - 50 and Col. 5, lines 12 – 14] and not a "rate" difference.

Applicant respectfully requests the Examiner to reconsider the prior indication of disagreement that the Dodd reference indicates that ""When the PLL is "locked", the frequency and phase of the output signal are the same as those of the input signal"

(Emphasis added) [Col. 5 lines 28 – 30]. Applicant respectfully asserts that the Dodd reference indicates the purpose of the PLL is to drive the VCO frequency in the direction of the input frequency and when "locked" the frequency of the output and input signal are the same [Col. 5 lines 27 –30]. Applicant respectfully asserts that the Dodd reference specifically indicates that the input and output frequencies are the same and are therefore can not necessarily be different.

Applicant respectfully asserts Claims 2 – 10, 12 – 16 and 18 - 20 are allowable as depending from an allowable independent Claims 1, 11 and 17 respectively.

With regard to Claim 2 and 3, the present Office Action realleges it is clear the system interface of the Dodd et al. reference communicates in series on one side and parallel on the other. To the extent the Dodd et al. reference may mention that the connection lines are represented as a single line to the buffer 120, and to the memory device 130 – 145, and each represented line may in fact be a plurality of lines [Col. 2 lines 54 –57], Applicant respectfully reasserts that Dodd et al. does not teach a system interface for communicating with a system controller at a first communication rate and a memory array interface for communicating with a memory array at a second communication rate, where said system interface comprises a serial read data port, a serial write data port and a serial address data port. Applicant also respectfully asserts the Dodd et al. reference does not mention serial information and/or a serial port. Applicant also respectfully reasserts that Dodd et al. does not teach a system array interface for communicating with a system controller at a first communication rate and a memory array interface for communicating with a memory array at a second communication rate, where said memory array interface comprises a parallel transmit

port, parallel receive port, a parallel address port and a control port. Applicant also respectfully asserts the Dodd et al. reference does not mention parallel information and/or a parallel port.

With respect to Claim 6, the present Office Action realleges the memory clock of the Dodd et al. reference is slower than the controller clock. To the extent the Dodd et al. reference may mention the input clock 10 is either driven from the memory controller 110 or from an external source [Col. 3 lines 67 – Col. 4 line 5], Applicant respectfully reasserts the Dodd et al. reference does not teach the memory array interface operates at a second clock speed that is slower than a first clock speed of operations at the system interface. In addition, Applicant respectfully reasserts the Dodd et al. reference teaches away from the present invention by indicating the input clock to the memory array is the same as the controller clock [Col. 3 lines 67 – Col. 4 line 5] and when the PLL is locked the frequency and phase of the output signal are the same as those of the input signal [Col. 5, lines 28 – 30].

With respect to Claim 7, the present Office Action makes a reference to "note" the address and control/command buses and data buses to and from memory devices (130/135 or 1-80). To the extent the Dodd et al. reference may show address and control/command buses and data buses to and from memory devices, Applicant respectfully reasserts the Dodd et al. reference does not teach a memory array interface deals with the reading and writing of data to and from a memory array with address and control buses as claimed in the present application.

With respect to Claims 13 and 14, the present Office Action realleges the advantages are irrelevant and do not define any step/structure that differs from the Dodd et al. reference. Applicant respectfully reasserts Claim 13 includes defined limitations including the single substrate is a well controlled environment and capacitive flux in the point to point connections is manageable. Applicant respectfully reasserts Claim 13 includes defined limitations including signals with low voltage swings that produce very low noise potential on each line.

With respect to Claims 11, 12, and 16 the present Office Action refers to the allegations discussed above. Applicant respectfully reasserts the Dodd et al. reference does not teach the present claimed invention as discussed above. The present Office Action also notes the Dodd et al. reference allegedly discloses a single chip memory module integrated high speed interface system. To the extent the Dodd reference may mention a buffer structure and memory devices are housed with in a memory module 150 [Fig. 5 and Col. 5, lines 60 – 65], Applicant respectfully reasserts the Dodd et al. reference does not teach a single chip memory module integrated high speed serial interface system comprising a memory module array and a high speed serial memory interface system as claimed in the present application. In addition, Applicant respectfully reasserts that the Dodd et al. reference teaches away from a single chip memory module by indicating the memory module 150 of the Dodd et al. reference is a board with separate memory devices 130 – 135 and separate buffer 120 [Fig. 2 and Col. 3, lines 20 – 45].

With regard to Claim 15 the present Office Action alleges the Dodd et al. reference teaches the data and address bits are provided synchronously upon a clock

signal edge. Applicant respectfully asserts the Dodd et al. reference does not teach data and address bits are provided synchronously upon a clock signal edge as claimed in the present application.

With regard to Claims 17 – 20, the present Office Action realleges it is clear that one using the system of the Dodd et al. reference would have performed the same steps set forth in claims 17 – 19. Applicant respectfully reasserts the Dodd et al. reference does not teach a high speed serial memory interface method as claimed in the present application.

103 Rejections

The present Office Action indicates Claims 8 and 10 are rejected under 35 U.S.C. 103 (a) as being unpatentable over the Dodd et al. reference. Applicant respectfully reasserts that the present invention is neither shown nor suggested by the Dodd et al. reference.

Regarding Claim 8, the present Office Action acknowledges that the Dodd et al. reference fails to teach double data rate (DDR). The present Office Action realleges that DDR clock is well known and it would have been obvious to one of ordinary skill in the art to use DDR. Even if the present Office Action allegation that DDR is well know is correct, Applicant respectfully reasserts a high speed serial memory interface system wherein communications are synchronous to a system clock at double rated clocking as claimed in the present application is not taught by the Dodd et al. reference nor obvious.

Regarding Claim 10, the present Office Action acknowledges that the Dodd et al. reference fails to teach an 8B/10B encoder. The present Office Action realleges that an 8B/10B encoder is well known and it would have been obvious to one of ordinary skill in the art to use an 8B/10B encoder. Even if the present Office Action allegation that a 8B/10B encoder is well know is correct, Applicant respectfully reasserts a high speed serial memory interface system including 8B/10B encoding as claimed in the present application is not taught by the Dodd et al. reference nor obvious.

ALLOWABLE SUBJECCT MATTER

The present Office Action indicates Claims 4 and 5 would be allowable is rewritten to include limitations of the base independent Claim. Applicant tanks the Examiner for indicating allowable subject matter. Applicant has cancelled Claims 4 and 5 without prejudice. Applicant has added new Claim 21 to incorporated the limitations of independent Claim 1 and cancelled Claim 4. Applicant has added new Claim 22 to incorporate the limitations of independent Claim 1 and cancelled Claim 5.

CONCLUSION

In light of the above remarks, Applicant respectfully requests allowance of the remaining Claims. The Examiner is urged to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

WAGNER, MURABITO & HAO

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